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Design of a planar Schottky diode based 200 GHz frequency multiplier

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***Abstract*— We present design of a 200 GHz frequency multiplier based on commercially available Schottky diodes. The device model has been extracted from millimeter-wave small-signal S-parameter measurements. The frequency multiplier is fully planar on alumina substrates. The resulting conversion efficiency is 18.9% at 96 GHz input frequency. The multiplier is contacted with the help of especially designed CPW to microstrip transitions.**

INTRODUCTION

The work presented here introduces MMIC-based multiplier and mixer circuits for THz frequencies. The work presented here employs simulation tools developed earlier [1], [2] to design a fully planar frequency multiplier with CPW feeds suitable for future implementation as an MMIC. Commercially available Schottky diodes from United Monolithic Semiconductors (UMS) have been used in the design, requiring special design and extra modelling effort. The parasitic model extraction is presented below together with the frequency multiplier circuit design.

DIODE MODELLING AND MULTIPLIER DESIGN

The full equivalent circuit for the UMS Schottky diode DBES105a is provided in fig.1 together with a comparison between the extracted model parameters and measured S-parameters. This device is comprised of two Schottky diodes in series. Both the amplitude and the

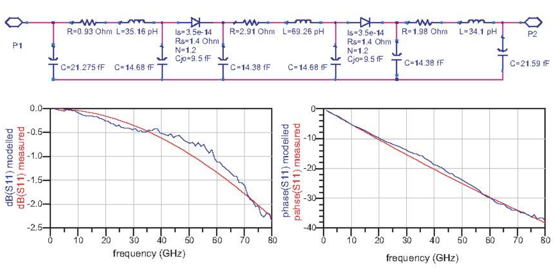

Fig. 1. Schottky diode equivalent circuit and comparison between the extracted circuit model of and measured small-signal S-parameters..

phase are well modelled over the frequency range.

It can be concluded that a very good agreement has been achieved between EM simulations and an equivalent circuit exhibiting parasitic elements. The access structure exhibits a resistance of the order of 1 Ω per diode together with a series inductance of around 30 pH. The capacitance modelling is a little more difficult, because the parasitic capacitance is distributed between the two contact access lines. A value of 14 fF and 21 fF have been found for the parasitic capacitances, respectively.

The device equivalent circuit was then used for the design of a frequency multiplier at an input frequency of 96 GHz. The frequency multiplier exhibits a conversion loss of around 18.9% with an output power of roughly 5.6 mW, at a dynamic DC current of 6mA. The bias was chosen to be $V_{bias} = -2V$. The fundamental impedance is $Z_{fund} = (19.5 + \jmath 64.2)\,\Omega$, while the impedance at the second harmonic is determined to be $Z_{2\cdot fund} = (23.56 + \jmath 46.5)\,\Omega$. These impedances take into account the parasitic effects stemming from the chip design.

The time-waveforms for the current and voltage across the diode for these conditions can be depicted in fig. **??** together with the layout of the frequency multiplier. Here one can depict the CPW contact pads with their transition to microstrip lines. There is a slight phase shift between the current and the voltage, which indicates that parasitic effects play an important role in this diode. A small asymmetry is also visible, but should not have a large impact on the device performance.

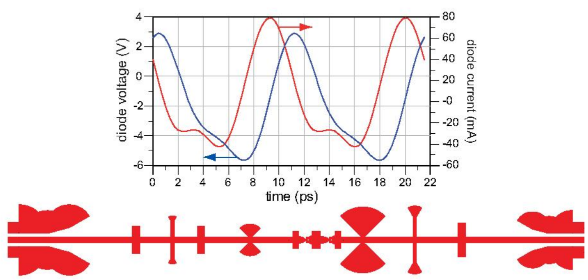

Fig. 2. Time waveforms for the diode voltage and current and the circuit topology for the frequency multiplier.

CONCLUSIONS

We show a successful design of a frequency multiplier based on commercial Schottky diodes in planar technology. Microstrip lines are employed in the circuit. The novel simulation tools developed earlier are employed in the design of the multiplier. The simulated results indicate a conversion efficiency of 18.9% with an output power of around 5.6mW at 192 GHz.

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